SCHEME OF INSTRUCTION AND EXAMINATION
B. E. (ECE)

V – Semester

SNo	Code	Course Title	Scheme of Instruction			Contact Hrs/ Wk	Scheme of Evaluation			Credits
			L	T	P		Hrs	CIE	SEE	
Theory										
1	PC501EC	Antennas and Wave Propagation	3	-	-	3	3	40	60	3
2	PC502EC	Digital System Design using Verilog HDL	3	-	-	3	3	40	60	3
3	PC503EC	Digital Communication	3	-	-	3	3	40	60	3
4	PC504EC	Linear Control Systems	3	-	-	3	3	40	60	3
5	PC505EC	Communication Theory	3	-	-	3	3	40	60	3
Practicals										
6	PC551EC	Analog and Digital Communication Lab	-	-	3	3	3	25	50	1.5
7	PC552EC	Digital System Design Lab	-	-	3	3	3	25	50	1.5
Total			**15**	**-**	**6**	**21**	**21**	**250**	**400**	**18**

Course Code	Course Title						Core//PE/OE
PC501EC	ANTENNAS AND WAVE PROPAGATION						Core
Pre-requisites	Contact Hours Per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	40	60	3

Course Objectives

1. To understand the various antenna parameters to give insight of the radiation phenomena
2. To have thorough understanding of radiation characteristics of different types of antennas.
3. To study the characteristics of array antennas having directional radiation characteristics
4. To get insight on aperture antennas and modern antennas
5. To understand the concepts of wave propagation and create awareness about the different types of propagation of radio waves at different frequencies

Course Outcomes

1. Acquires knowledge about the basic antenna parameters and radiation concepts
2. Analyze wire antennas in detail
3. Attain engineering fundamentals to analyze and design antenna arrays
4. Classify, analyze and design aperture and modern antennas
5. Identify and explain modes of propagation in different regions of atmosphere

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	-	-	-	-	-	-	-	-	-	-		
CO2	2	3	-	-	-	-	-	-	-	-	-	-		
CO3	3	-	3	-	1	1	1	1	-	-	-	-		
CO4	2	2	-	-	-	1	-	-	1	-	-	1		
CO5	2	2	-	-	-	-	1	1	-	-	-	-		

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT–I

Fundamentals of Antenna theory: Principle of radiation, Basic Antenna Parameters – Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity, Gain, Antenna Apertures, Effective Height, Illustrative Problems. Retarded Potentials – Helmholtz Theorem. Thin Linear Wire Antennas – Radiation from Small Electric Dipole, Quarter Wave Monopole and Half Wave Dipole – Current Distributions, Near field and Far field Components, Radiated Power, Radiation Resistance, Beam Width, Directivity, Effective Area and Effective Height. Loop Antennas – Introduction, Small Loop, Comparison of Far Fields of Small Loop and Short Dipole.

UNIT–II

Antenna Arrays: Basic two element array, N element uniform linear array, Pattern multiplication, Broadside and End fire array, Planar array, Concept of Phased arrays, Basic principle of antenna Synthesis-Binomial array, Tschebysev array.

UNIT–III

Practical Antennas: Yagi-Uda antenna, V-Antenna, Rhombic antenna, Travelling wave antennas, Microstrip antennas– Introduction, Features, Advantages and Limitations, Rectangular Patch Antennas – Geometry, Design equations and Characteristics.

UNIT-IV

Aperture and Modern Antennas: - Reflector Antennas – Introduction, Flat Sheet and Corner Reflectors, Paraboloid Reflectors – Geometry, Pattern Characteristics, Feed Methods, Reflector – Types, Related Features, Illustrative Problems. Horn Antennas – Types, Fermat's Principle, Radiation from sectoral and pyramidal horns, Design Considerations of Pyramidal Horns, Reconfigurable antenna, Active antenna, Dielectric Antennas, Electronic band gap structure and applications.

UNIT – V

Wave propagation: Ground wave propagation. Space and surface waves, Tropospheric refraction and reflection. Sky wave propagation – Virtual height, critical frequency, Maximum usable frequency – Skip distance, Fading, Multi-hop propagation.

SUGGESTED READING:

1 Constantine A. Balanis, Modern Antenna Handbook, A John Wiley & Sons, Inc., Publication, 2008.

2 John D.Kraus, Ronald J.Marhefka and Ahmed S.Khan, Antennas for All Applications, 3rd Edition, Tata McGraw- Hill publishing company Limited, New Delhi, 2006.

3 K.D.Prasad, "Antennas and Wave Propagation", Khanna or Satya Publications.

4 Warren L. Stutzman, Gary A. Thiele, Antenna Theory and Design, 3rd Edition. May 2012

Course Code	Course Title						Core//PE/OE
PC502EC	DIGITAL SYSTEM DESIGN USING VERILOG HDL						Core
Pre-requisites	Contact Hours Per Week				CIE	SEE	Credits
	L	T	D	P			
STLD	3	-	-	-	40	60	3

Course Objectives: The course is taught with the objectives of enabling the student to:

1. Familiarize with structural modeling with different design approaches and writing test
2. Familiarize with behavioral modeling of digital systems using Verilog HDL
3. Understand synthesis of various sub systems
4. Familiarize with various ICs available (combinational units) and their usage and to design
5. Understand FSM coding

Course Outcomes : On completion of this course, the student will be able to :

1. Develop structural designs in top-down and bottom-up approach and develop test benches for the same
2. Develop combinational and sequential circuits in data flow and behavioral modeling styles
3. Understand the various language constructs and the corresponding hardware implementation (Synthesis).
4. Familiarize with commercially available ICs of various combinational and sequential building blocks
5. Develop verilog code for FSMs and FSMDs and verify

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	2	1	2	-	-	-	1	-	-	-	2	-
CO2	2	1	2	2	2	-	-	-	1	-	-	-	2	-
CO3	2	2	1	2	1	-	-	-	-	-	-	-	2	-
CO4	2	2	1	1	-	-	-	-	-	-	-	1	1	-
CO5	2	1	1	1	3	-	-	-	1	-	-	1	1	-

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT–I

INTRODUCTION TO LOGIC DESIGN WITH VERILOG: Structural models of combinational logic: Verilog primitives, design encapsulation, structural models, module ports and structural connectivity, Top-down and nested modules, design hierarchy, vectors in Verilog. Four valued logic and signal resolution in Verilog, test methodology, Signal generators for test

benches, test bench templates, propagation delay and truth table models of Combinational and sequential logic with Verilog.

UNIT–II LOGIC DESIGN WITH BEHAVIORAL MODELS OF COMBINATIONAL AND

SEQUENTIAL LOGIC: Data types, continuous assignment, Boolean equation based behavioral models of combinational logic-multiplexers, encoders, decoders, modeling flip-flops and latches, edge detection, LFSRs, Modeling with repetitive algorithms(loops), clock generators, behavioral models of counters, registers, register files and Array of registers(Memories)

UNIT–III SYNTHESIS OF COMBINATIONAL AND SEQUENTIAL LOGIC - Introduction to

synthesis - Logic synthesis, RTL synthesis, High-level synthesis, Synthesis of combinational logic, synthesis of sequential logic with latches and flip flops, synthesis of loops.

Introduction to VLSI RTL designs: RTL designs- Goals and Constraints, RTL based chip design flow and design challenges

UNIT-IV

COMBINATIONAL LOGIC ICS – Specifications and Applications of TTL-74XX MSI ICs - Decoders, BCD- seven segment display Decoders with Drivers, Encoders, Priority Encoders, Multiplexers, Parity Generators/Checkers, Parallel Binary Adder/Subtractor and Magnitude Comparators

SEQUENTIAL LOGIC IC'S: Familiarity with commonly available TTL 74XX, CMOS 40XX Series ICs – Asynchronous and synchronous Counters, Decade Counters, Shift Registers.

UNIT – V

FINITE STATE MACHINES: Introduction, Mealy and Moore Outputs, FSM representationstate diagram and ASM chart, FSM code development and design examples.

FSM WITH DATA PATH (FSMD): Introduction, single RT operation, ASMD chart , Decision box realization with register, code development for FSMD with design examples.

SUGGESTED READING:

1. Michael D. Ciletti , "Advanced digital design with Verilog HDL", PHI learning Pvt Ltd, 2012
2. Samir Palnitkar, *"Verilog HDL A Guide to Digital Design and Synthesis,"* 2nd Edition, Pearson Education, 2006.
3. Sanjay Churiwala · Sapan Garg "Principles of VLSI RTL design- A practical guide", , Springer, 2010
4. R.P.Jain, *"Modern Digital Electronics",* Tata McGraw Hill, 4th Edition, 2009.
5. Pong P Chu, "FPGA Proto Typing by Verilog Examples" WILEY Publications

Course Code	Course Title						Core//PE/OE
PC503EC	**DIGITAL COMMUNICATION**						**Core**
Pre-requisites	**Contact Hours Per Week**				**CIE**	**SEE**	**Credits**
	L	**T**	**D**	**P**			
Analog Communication, Probability Theory and Stochastic Process	3	-	-	-	40	60	3

Course Objectives: The course is taught with the objective of enabling the student to

1. Understand the building blocks of digital communication systems and waveform coding techniques
2. Get familiarized with various source coding techniques and Block codes
3. Get familiarized with convolution and cyclic codes
4. Analyze various digital carrier modulation techniques
5. Understand the concept of spread spectrum modulation

Course Outcomes : On completion of this course, the student will be able to :

1. Understand the basic components of digital communication systems
2. Understand how to design block codes, convolution, and cyclic codes
3. Apply suitable digital carrier modulation techniques and coding techniques for various applications for improved spectral efficiency
4. Learn to design an optimum receiver and analyze the error performance of baseband and band pass data transmission
5. Analyze the performance of the spread spectrum communication system

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	1	3	1	-	-	-	-	-	1	2
CO2	2	2	1	3	2	-	-	-	-	-	1	1
CO3	2	2	1	3	3	-	-	-	-	-	1	1
CO4	2	2	1	3	3	-	-	-	-	-	2	1
CO5	3	2	1	3	3	-	-	-	-	-	2	1

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT–I

Digital Transmission of Analog Signals: Elements of digital communication system, Sampling theory, Quantizing of Analog Signals, Coded Transmission of Analog Signals: PCM, Differential PCM, Delta Modulation, Noise in PCM, DM system. Performance comparison of the above systems.

UNIT–II

Source Coding: Introduction, Shannon-Fano Coding, Huffman Coding.

Linear Block Codes: Introduction, Matrix description of Linear Block codes, Error Detection and Error Correction capabilities of linear block codes, Single Error Correcting Hamming codes.

UNIT–III

Binary Cyclic Codes: Algebraic Structure of Cyclic Codes, Encoding, Syndrome Calculation, , Error Detection and Error Correction, BCH Codes

Convolution Codes: Introduction, Encoding of convolution codes, Graphical approach: State, Tree and Trellis diagram, The Viterbi algorithm. Comparison of the above codes.

UNIT-IV

Digital Band-Pass Modulation Techniques: Binary Amplitude-Shift Keying, Phase-Shift Keying, Frequency-Shift Keying, Summary of Three Binary Signaling Schemes, Noncoherent Digital Modulation Schemes, M-ary Digital Modulation Schemes, Mapping of Digitally Modulated Waveforms onto Constellations of Signal Points.

Bit Error Rate, Detection of a Single Pulse in Noise, Optimum Detection of Binary PAM in Noise, Optimum Detection of BPSK, Detection of QPSK and QAM in Noise, Optimum Detection of Binary FSK.

UNIT – V

Spread Spectrum Modulation: Introduction, Generation and Characteristics of PN- sequences. Direct Sequence Spread Spectrum system; Frequency Hopping spread spectrum system and their application, acquisition scheme for spread spectrum receivers, tracking of FH and DS signals.

SUGGESTED READING:

1. K Sam Shanmugam, *"Digital and Analog Communication Systems*", John Wiley &sons, 1979.
2. John G. Proakis, *"Digital Communications*", 4thEdition, Tata McGraw- Hill Publishing Company Limited, New Delhi, 2003.
3. Rodger E.Ziemer, William H.Tranter, "Principles of Communications-Systems, Modulation and Noise", 7th Edition,Wiley,2014.

Course Code	Course Title						Core//PE/OE
PC504EC	LINEAR CONTROL SYSTEM						Core
Pre-requisites	Contact Hours Per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	40	60	3

Course Objectives : The course is taught with the objectives of enabling the student to:

1. To develop mathematical modeling for different control systems
2. To construct state space model for continuous and discrete data systems and analyze them
3. To analyze control system in time domain and determine stability using Routh-Hurwitz criterion and Root-Locus technique
4. To analyze control system in frequency domain and determine stability using Nyquist criterion and bode plots
5. To design compensators for control systems

Course Outcomes : On completion of this course, the student will be able to :

1. Able to develop mathematical models and derive transfer functions for various systems
2. Able to expose to an appropriate state space modeling of system and its analysis and the concept and testing of controllability and observability
3. Able to analyze the systems in time domain and determine its stability
4. Able to analyze the systems in frequency domain and determine relative stability 5. Able to design compensators for a given specifications

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	3	-	1	1	-	-	-	-	1	2	3	-
CO2	1	1	3	0	-	-	-	-	-	-	-	2	3	3
CO3	3	3	3	1	1	1	-	-	-	-	-	1	3	3
CO4	2	2	3	1	-	-	-	-	-	-	2	1	3	-
CO5	1	1	2	-	-	-	-	-	-	-	2	2	3	3

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT–I

Introduction to control systems: Basic components, classification of control systems, effects of feedback, mathematical modeling of physical systems, - Mathematical modelling of control systems - Electrical Systems and mechanical translational systems - transfer function – Electrical analogous of mechanical translational and Rotational systems -Block diagrams representation and reduction methods - signal flow graph - mason's gain formula

UNIT–II

State-variable analysis of continuous data systems: state, state variables, state equations, solution of state equations, state transition matrix and its properties, state diagram, relationship between state equations and transfer functions, concept and testing of controllability and observability.

UNIT–III

Analysis of continuous time systems - time domain solution of first order systems – time constant, time domain specifications - time domain solution of second order systems – damping ratio - response of second order systems for step input - steady state error and static error coefficients for standard inputs - concept of stability –location of roots on the s plane - Routh-Hurwitz techniques - construction of root locus

UNIT-IV

Frequency-domain analysis: Introduction to Frequency domain specifications, Relationship between time and frequency response, Nyquist stability criterion, Bode plots, relative stability – gain margin and phase margin.

UNIT – V

Design of control systems: Phase lag, phase lead and phase Lag-Lead compensators and their design. Controllers: Introduction to PI, PD and PID controllers.

SUGGESTED READING:

1. I.J.Nagrath and M Gopal, “Control System Engineering”, New Age International Private Limited, New Delhi, 2008, 5th Edition
2. Katsuhiko Ogata, “Modern Control Engineering”, Prentice-Hall of India Private Limited, New Delhi, 2003, 4th Edition.
3. Benjamin C. Kuo, “Automatic Control Systems”, Prentice Hall of India, 2009, 7th Edition
4. Control Systems Engineering by A. Nagoor Kani, RBA Publications

Course Code	**Course Title**				**Core/PE/OE**	
PC 505 EC	**COMMUNICATION THEORY**				**Core**	
Pre-requisites	-		**L**	**T**	**P**	**C**
			3	-	-	3
Evaluation	**SEE**	60 Marks	**CIE**		40 Marks	

Course Objectives:	
The course is taught with the objectives of enabling the student to:	
1	To understand the concept of modulation and linear modulation techniques.
2	To understand the angle modulation schemes and characteristics of transmitters and receivers.
3	To study the types of noise and influence analog modulation.
4	To understand the Pulse Analog modulation schemes
5	To interpret the principles of information theory

Course Outcomes:	
On completion of this course, the student will be able to :	
CO-1	Able to compare the performance of AM, FM and PM schemes with reference to band width. Understand generation of AM, FM, PM schemes.
CO-2	Able to evaluate the performance of AM and FM transmitters and receivers.
CO-3	Able to identify sources of noise, noise figure, signal to noise ratio for AM, FM and PM.
CO-4	Understand the concept of pulse modulation and compare their performance.
CO-5	Able to acquire knowledge about information theory and access entropy and efficiency of various channels.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	2	1	2	-	-	-	2	-	-	1	1
CO2	3	2	2	2	1	2	-	-	-	2	-	-	1	1
CO3	3	3	2	2	1	2	-	-	-	2	-	-	1	1
CO4	3	2	2	2	1	2	-	-	-	2	-	-	2	1
CO5	3	2	2	2	1	2	-	-	-	2	-	-	2	2

Correlation rating : Low / Medium / High : 1 / 2 / 3 respectively.

UNIT - I

Linear modulation schemes: Need for modulation, double-sideband suppressed-carrier (DSBSC) modulation, conventional amplitude modulation (AM), single side band (SSB) modulation and vestigial-sideband (VSB) modulation. Generation and demodulation of the above, Frequency Division Multiplexing.

UNIT – II

Angle modulation schemes: frequency modulation (FM) and phase modulation (PM), conceptofinstantaneousfrequency,NBFM,WBFM,FMspectrumintermsofBesselfunction, direct and indirect (Armstrong‟s) methods of FM generation, discriminators, phase locked loop (PLL), FM receiver.

AM and FM radio transmitters, Principles of tuned radio frequency (TRF) and super heterodyne receivers, choice of intermediate frequency (IF).

UNIT - III

Noise performance of AM, FM and PM systems: Sources of noise, thermal noise, shot noise, noise in linear systems, equivalent noise band width, noise temperature, noise figure.
Signal-to noise ratio (SNR) calculations for DSB-SC AM,SSB, FM and PM systems.

UNIT – IV

Analog Pulse modulation schemes: sampling of continuous-time signals, low pass and band pass sampling, practical aspects of sampling and reconstruction of signals. Pulse amplitude modulation (PAM), Time Division Multiplexing, Pulse time modulation schemes-pulse width modulation(PWM)and pulse position modulation(PPM), generation and demodulation

UNIT - V
Information Theory: Introduction, Information entropy, properties of entropy, information rate, types of information sources, channels, types of channels, joint entropy, conditional entropy, redundancy, mutual information, channel capacity

Suggested Reading:

1	K Sam Shanmugam, *"Digital and Analog Communication Systems*", John Wiley & sons, 1979.
2	JohnG.Proakis,*"DigitalCommunications*",4thEdition,TataMcGrawHillpublishingcompanyLimited, New Delhi, 2003
3	PRamakrishnaRao,"*DigitalCommunication*",TataMcGraw-HillEducationPrivate Limited, New Delhi, 2011.

Course Code	Course Title						Core//PE/OE
PC551EC	**ANALOG AND DIGITAL COMMUNICATION LAB**						**Core**
Pre-requisites	**Contact Hours Per Week**				**CIE**	**SEE**	**Credits**
Analog and Digital Communications	**L**	**T**	**D**	**P**			
	-	-	-	2	25	50	1

Course Objectives : The course is taught with the objectives of enabling the student to:

1. Perform Analog modulation and demodulation techniques and measure modulation
2. Perform experiments on Radio Receivers to measure their performance parameters
3. Perform Pulse analog modulation and demodulation techniques and understand.
4. Perform Pulse digital modulation and demodulation techniques and understand.
5. Perform carrier modulation techniques

Course Outcomes : On completion of this course, the student will be able to :

1. Acquire knowledge of performing modulation and demodulation and analyze the effects of various parameters on the process
2. Acquire knowledge of operation of various radio receiver sub systems
3. Acquire in-depth understanding of pulse analog modulation techniques
4. Acquire in-depth understanding of pulse digital modulation Techniques 5. Acquire skill to perform carrier modulation

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO	2	1	-	1	-	-	-	-	-	-	-	-
1CO	1	1	-	1	-	-	-	-	-	-	-	-
2CO	2	1	-	1	-	-	-	-	-	-	-	-
3CO	1	1	-	1	-	-	-	-	-	-	-	-
4CO	2	-	-	-	-	-	-	-	-	-	-	-

5Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

Experiment–I

To study the function of Amplitude Modulation & Demodulation (under modulation, perfect modulation & over modulation) and calculate the modulation index

Experiment–II

To study the functioning of frequency modulation & demodulation

Experiment–III

To observe the characteristics of a Frequency Mixer and to measure its conversion gain

Experiment–IV
To Study the AGC characteristics of a Radio Receiver

Experiment–V
To Study Pulse Amplitude Modulation and Demodulation

Experiment–VI
To Study Pulse Width Modulation and Demodulation using different sampling frequency

Experiment–VII
To study and observe the operation of Phase Lock Loop and its Capture range, lock range free running VCO Frequency

Experiment–VIII
To analyze a PCM system and interpret the modulated and demodulated waveforms.

Experiment–IX
To Study the Delta Modulation process by comparing the present signal with the previous signal of the given modulation signal and Demodulate the same

Experiment–X
To Study the ASK, FSK, PSK, QPSK Modulator and Demodulator and interpret the modulated and demodulated waveforms, and plot BER using MATLAB

SUGGESTED READING:

1 Simon Haykin*, "Communication Systems",* 4th Edition, John Wiley &sons.inc, 2000.

2 George Kennedy, Bernard Davis, *"Electronic Communication Systems"*, 4th Edition, Tata McGraw-Hill publishing company Limited, New Delhi, 1993.

Course Code	Course Title						Core//PE/OE
PC552EC	DIGITAL SYSTEM DESIGN LAB						Core
Pre-requisites	Contact Hours Per Week				CIE	SEE	Credits
Switching theory and logic design	L	T	D	P			
	-	-	-	2	25	50	1

Course Objectives : The course is taught with the objectives of enabling the student to:

1. To understand the operation of basic combinational building blocks
2. Understand the operation of display devices and perform code conversions
3. Understand the operation of all Flip flops
4. Design combinational and sequential circuits for given applications
5. Understand and design counters and registers using basic building blocks **Course Outcomes :** On completion of this course, the student will be able to : 1. Use all basic building blocks to design any combinational functions
2. Configure and use display devices
3. Use all flip flops in sequential design and convert flip flops from one form to another
4. Use and configure IC counters as per the given specification
5. Design resisters and use them as per the application

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	2	-	-	1	-	-	3	2	-	1	1	-
CO2	2	2	2	-	-	1	-	-	3	2	-	1	1	-
CO3	2	2	2	-	-	2	-	-	3	2	-	1	1	-
CO4	2	2	2	1	-	2	-	-	3	2	-	1	2	-
CO5	2	2	2	1	1	2	-	-	3	2	-	1	2	-

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

Experiment -I

Verification of all basic gates using universal gates

Experiment –II

TTL combinational gate applications: Design and verify

1. 4-bit Binary to Grey code converter
2. AOI gate using 7400IC
3. Full adder and Full Subtractor
4. Full adder using 4:1 Mux

Experiment –III

Verify the operation of BCD- &-segment Decoder (7447) using 7-segment LED display

Experiment –IV

Verify the function of all flip flops realized using basic gates (SR, JK, T and D)

Experiment –V

Convert JK flip flop into T and D Flip flops and verify the design (use basic gates)

Experiment –VI

Design and verify a 3-bit up/down counter

Experiment –VII

Configure IC 7483 as BCD adder and verify the design

Experiment –VIII

Verify the operation of decade counter using IC 7490, configure it as Mod-N (N<9) counter and verify the operation

Experiment –IX

Configure IC 7492 as divide by 3 and 6 counter and verify

Experiment –X

Construct a 4-bit shift register (SISO) using IC 7476 and other logic gates and verify the operation

Experiment –XI

Design and verify the following using Verilog HDL

1. 8:1 encoder using structural modeling
2. BCD – 7-segment decoder using conditional constructs
3. 8:1 Encoder using behavioral constructs
4. ALU using Case Construct
5. 3-bit Binary counter using Loop statements

SUGGESTED READING:

1. R.P.Jain, “Modern Digital Electronics”, Tata McGraw Hill, 4th Edition, 2009
2. M.Morris Mano, Michael D. Ciletti, “Digital Design”, Pearson, 4th Edition, 2012
3. Ming-Bo Lin, “Digital System Design and Practices Using Verilog HDL and FPGAs”, Wiley India Pvt. Ltd., 2012

SCHEME OF INSTRUCTION AND EXAMINATION
B. E (ECE)

VI – Semester

S. No	Code	Course Title	Scheme of Instruction			Contact Hrs/Wk	Scheme of Evaluation			Credits
			L	T	P		Hrs	CIE	SEE	
Theory										
1	PC601EC	Microcontrollers and Interfacing	3	-	-	3	3	40	60	3
2	PC602EC	Data Communications and Computer Networks	3	-	-	3	3	40	60	3
3	PC603EC	Embedded System Design	3	-	-	3	3	40	60	3
4	PC604EC	VLSI Design	3	-	-	3	3	40	60	3
5		**Professional Elective-I**	3			3	3	40	60	3
		PE611EC Python Programming								
		PE612EC Operating Systems								
		PE613ECS Data Science Using R								
Practicals										
6	PC651EC	Electronic Design Automation Lab	-	-	3	**3**	3	25	50	1.5
7	PC652EC	Microcontrollers Lab	-	-	3	**3**	3	25	50	1.5
8	PW653EC	Mini-Project	-	-	6	**6**	-	50	-	3
Total			**15**	**-**	**12**	**25**	**21**	**300**	**400**	**21**

SCHEME OF INSTRUCTION AND EXAMINATION
B. E (ECE)
VI – Semester

Course Code	Course Title						Core//PE/OE
PC601EC	**MICRO-CONTROLLERS AND INTERFACING**						**Core**
Pre-requisites	**Contact Hours Per Week**				**CIE**	**SEE**	**Credits**
Computer Organization, Micro Processors	**L**	**T**	**D**	**P**			
	3	-	-	-	40	60	3

Course Objectives : The course is taught with the objectives of enabling the student to:

1. Discuss 8051 Basic architecture and programming
2. Discuss Timers, serial communication and interrupts of 8051
3. Discuss ARM architecture and Programming
4. Discuss Real time Interfacing and Programming

Course Outcomes : On completion of this course, the student will be able to :

1. To gain a comprehensive understanding of the 8051 microcontroller architecture and develop practical skills in programming
2. Understand timers, serial communication, and interrupts in embedded systems, along with practical skills in programming these features on the 8051 microcontroller
3. Understand RISC based ARM architecture
4. Develop programs for basic problem solving
5. Develop real time interfacing using 8051 and ARM

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	1	1	-	-	-	-	-	-	-	-	-	1
CO2	2	2	1	1	-	-	-	-	-	-	-	1
CO3	2	2	1	1	-	-	-	-	-	-	-	1
CO4	2	3	3	3	-	1	-	-	-	-	-	1
CO5	2	3	3	3	-	2	-	-	-	-	-	1

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT–I

8051 Architecture and Programming:

Evolution of Microprocessors and Microcontrollers, Programming model of 8051, Register Organization, Flag Register, Pin configuration, Memory Organization: ROM and RAM, Register Bank, Addressing modes and Instruction Set. Assembly Language Programming and C programming. Internal structure of Ports and alternate functions of Ports, 8051 I/O programming, bit manipulation programs using I/O ports

UNIT–II

Timer, Serial communication and Interrupt programming:

Concept of Timer, Programming model of Timers of 8051, Programming timers, Basics of Serial Communication, Serial communication standards, Programming model of UART of 8051, Concept of Interrupts, 8051 Interrupts, Programming Interrupts.

UNIT–III

ARM-CORTEX-M: General Description, Features, Cortex M Architecture, Block Diagram, Registers, Reset, Memory, Operating Modes. Introduction to Input /Output

UNIT-IV

ARM Cortex-M Instruction Sets and Programming: The Software Development Process, ARM Cortex-M Assembly Language Syntax, Addressing Modes, Operands, Memory Access Instructions, Logical, Shift, Arithmetic Operations, Stack, Functions and Control Flow, Assembler Directives.

UNIT – V

Interfacing with 8051: D/A converter, A/D converter, multiplexed key board, multiplexed seven segment display, LCD interfacing, stepper Motor interfacing,
Interfacing with ARM Controller
I/O Port Programming and Direction Register, Switch inputs and LED outputs, PLL, Sys Tick Timer, PWM, Communication Interfaces.

SUGGESTED READING:

1. Mohammad Ali Mazidi, Rolin D McKinley, Janice G Mazidi, The 8051 Microcontroller and Embedded Systems, Second Edition, Prentice Hall
2. Raj Kamal, Embedded Systems – Architecture, Programming and Design, 2nd Edition, TMH, 2008
3. Jonathan W Valvano, INTRODUCTION TO ARM®CORTEX-M MICROCONTROLLERS Volume 1, Fifth Edition June 2014
4. Dr. Yifeng Zhu , Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C
5. Kenneth J Ayala, The 8051 Micro Controller: Architecture, Programming and Applications.

Course Code	Course Title						Core//PE/OE
PC602EC	DATA COMMUNICATIONS AND COMPUTER NETWORKS						Core
Pre-requisites	Contact Hours Per Week				CIE	SEE	Credits
	L	T	D	P			
Computer Organization	3	-	-	-	40	60	3

Course Objectives : The course is taught with the objectives of enabling the student to:

1. To provide a conceptual foundation for the study of data communications using the Open Systems Interconnect (OSI) model for layer architecture
2. To study the principles of network protocols and Internet working
3. To understand the Network security and Internet applications
4. To understand the concepts of switched communication networks
5. To understand the performance of data link layer protocols for error and flow control and network security

Course Outcomes : On completion of this course, the student will be able to :

1. Understand the working of various network topologies, circuit and packet switching
2. Comprehend the role of data link layers and significance of MAC protocols
3. Understand the networking protocols and Internet protocols
4. Understand the transport layer working with TCP, UDP and ATM protocols
5. Comprehend the functionality of application layer and importance of network security

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	3	1	-	-	-	-	-	1	2
CO2	2	2	1	3	2	-	-	-	-	-	1	1
CO3	2	2	1	3	3	-	-	-	-	-	1	1
CO4	2	2	1	3	3	-	-	-	-	-	2	1
CO5	3	2	1	3	3	-	-	-	-	-	2	1

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT–I

Data communication: A Communication Model, The Need for Protocol Architecture and Standardization, Network Types: LAN, WAN, MAN. Network Topologies: Bus, Star, Ring, Hybrid. Line configurations. Reference Models: OSI, TCP/IP.

Circuit switching: Circuit Switching Principles and concepts.

Packet switching: Virtual circuit and Datagram subnets, X.25.

UNIT–II

Data Link Layer: Need for Data Link Control, Design issues, Framing, Error Detection and Correction, Flow control Protocols: Stop and Wait, Sliding Window, ARQ Protocols, HDLC.
MAC Sub Layer: Multiple Access Protocols: ALOHA, CSMA, Wireless LAN. IEEE 802.2, 802.3, 802.4, 802.11, 802.15, 802.16 standards. Bridges and Routers.

UNIT–III

Network Layer: Network layer Services, Routing algorithms: Shortest Path Routing, Flooding, Hierarchical routing, Broadcast, Multicast, Distance Vector Routing, and Congestion Control Algorithms
Internet Working: The Network Layer in Internet: IPV4, IPV6, Comparison of IPV4 and IPV6, IP Addressing, ATM Networks

UNIT-IV

Transport Layer: Transport Services, Elements of Transport Layer, Connection management, TCP and UDP protocols, ATM AAL Layer Protocol.

UNIT – V

Application Layer: Domain Name System, SNMP, Electronic Mail, World Wide Web.
Network Security: Cryptography Symmetric Key and Public Key algorithms, Digital Signatures, Authentication Protocols.

SUGGESTED READING:

1. Andrew S Tanenbaum, “Computer Networks,” 5/e, Pearson Education, 2011.
2. Behrouz A. Forouzan, “Data Communication and Networking,”3/e, TMH, 2008.
3. William Stallings, “Data and Computer Communications,” 8/e, PHI, 2004.
4. Douglas E Comer, “Computer Networks and Internet”, Pearson Education Asia, 2000.
5. Prakash C. Gupta, “Data Communications and Computer Networks”, PHI learning,2013

Course Code	Course Title						Core//PE/OE
PC603EC	EMBEDDED SYSTEM DESIGN						Core
Pre-requisites	Contact Hours Per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	40	60	3

Course Objectives : The course is taught with the objectives of enabling the student to:

1. To understand the processor selection criteria for Embedded System Design.
2. To provide a clear understanding of role of firmware, operating systems in correlation with hardware systems.
3. To gain the knowledge of tool chain for embedded systems.
4. To understand the importance of RTOS in building real time systems **Course Outcomes :** On completion of this course, the student will be able to :

1. Design an embedded system.
2. Distinguish between RISC and CISC
3. Design procedure of embedded firm ware
4. Use Embedded Software Development Tools for Designing Embedded System applications
5. Apply their understanding in building real time systems

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	1	-	-	-	1	-	1	1	1	1	3
CO2	3	1	2	2	-	1	-	1	-	2	1	1	1	3
CO3	3	1	2	2	1	1	-	1	--	2	1	1	1	3
CO4	3	1	2	1	1	1	-	1	-	1	1	1	1	3
CO5	3	2	2	1	-	1	-	1	-	1	1	1	1	3

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT–I

Introduction to Embedded Systems: Embedded systems Vs General computing systems, History of Embedded systems, classification, Characteristics and quality attributes of Embedded Systems Challenges in Embedded System Design, Application and Domain specific Embedded Systems.

UNIT–II Embedded firmware and Design and Development: Embedded Firmware Design Approaches and Development languages and Programming in Embedded C

UNIT–III

Embedded Software Development Tools: Host and Target Machines, Cross Compilers, Cross

Assemblers, Tool Chains, Linkers/Locators for Embedded Software, Address Resolution, Locator Maps. Getting Embedded Software Into Target System: PROM programmer, ROM emulator, In Circuit- Emulators, Monitors, Testing on Your Host Machine - Instruction Set Simulators, Logic Analysers.

UNIT-IV

Introduction to Real Time Operating Systems: Tasks and task states, tasks and Data, Semaphores and shared data. Operating system services: Message queues, mailboxes and pipes, timer functions, events, memory management, Interrupt routines in an RTOS environment..

UNIT – V

TASK COMMUNICATION: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

SUGGESTED READING:

1. Shibu KV, Introduction to Embedded System, Mc-Graw Hill, 2010.
2. Raj Kamal, Embedded Systems Architecture, Programming and Design, 2nd Ed., McGraw Hill, 2010
3. An Embedded Software Primer - David E. Simon, Pearson Education.
4. Jean.J.Labrosse, *MicroC/OS-II*, Taylor & Francis, 2002

Course Code	Course Title						Core//PE/OE
PC604EC	VLSI DESIGN						Core
Pre-requisites	Contact Hours Per Week				CIE	SEE	Credits
	L	T	D	P			
ED, STLD and DSDHDL	3	-	-	-	40	60	3

Course Objectives : The course is taught with the objectives of enabling the student to:

1. To provide a perspective on Digital Design in the Deep Sub-micron Technology
2. To focus on CMOS and Bi CMOS Short-channel Transistor Models
3. To Study CMOS Inverter elaborately
4. To explore static and dynamic implementations of combinational and sequential circuit designs
5. Introduce Testability of VLSI circuits

Course Outcomes : On completion of this course, the student will be able to :

1. Have an understanding of the Fabrication processes and the comparison between different state-of-the-art CMOS technologies
2. Acquire the knowledge in understanding CMOS Inverter characteristics. Illustrate circuit diagrams, stick diagrams and layouts
3. Design and analyze various Combinational Logic circuits in different models
4. Design and analyze various Arithmetic Blocks and Memory structures
5. Understand various fault models and testing methods

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	-	-		-	-	-	-	1	-	-	1	-	-
CO2	3	2	2	1	-	-	-	-	2	-	-	-	1	-
CO3	3	2	2	1	-	-	-	-	2	-	-	-	2	-
CO4	3	2	-	1	-	-	-	-	2	-	-	1	-	-
CO5	3	1	1		-	-	-	-	1	-	-	1	2	-

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT–I

Design Abstraction in Digital circuits, Fabrication process flow of NMOS and PMOS transistors, Overview of CMOS and BiCMOS technologies, MOSFET Transistor under static conditions, channel Length Modulation, Velocity Saturation, Sub-threshold Condition, Threshold variations, MOS structure Capacitance, CMOS Latch up, Technology scaling

UNIT–II

Digital CMOS Design: Static CMOS inverter-switching threshold, Noise margins, Voltage Transfer Characteristics, CMOS inverter Dynamic behavior- computing capacitance and propagation delay, Static and Dynamic Power Consumption.

Complementary CMOS, Ratioed Logic, Pass Transistor Logic, Full Adder and carry save multiplier design Considerations, Dynamic CMOS design -basic principle, Signal integrity issues in Dynamic Design, cascading dynamic gates. Designing sequential logic circuit-Bistability Principle, Multiplexer based latch, Dynamic latches and registers

UNIT–III

Analog CMOS design: Significance of analog integrated circuits, Suitability of CMOS for analog IC design, , biasing styles, single stage amplifier with resistive load, single stage amplifier with diode connected load, CS, CD, CG amplifiers, current sources and sinks, limitations of single stage amplifier, gain boosting techniques, current mirror principles, introduction to differential amplifier

UNIT-IV

Designing Memory and Array architectures: Memory classification, Architecture and building blocks, Memory Core-Rom, Non volatile RWM, RAM-Static RAM, Dynamic RAM, Memory Peripheral Circuitry-Address decoders-Row decoders-static and dynamic, column and block decoders, sense amplifiers-differential and single ended sensing, voltage references, Timing and control.

UNIT – V

Implementation of strategies for Digital ICs, Testing of VLSI circuits**:** VLSI Chip Yield, Test procedures; Design for Testability- Ad Hoc Testing, Scan Based testing, Boundary Scan Design, Built in Self-Test, Built-in logic block observer, Test Pattern Generator, Automatic Test Pattern Generation (ATPG)

SUGGESTED READING:

1. JAN.M. Rabaey, A. Chandrakasan and B. Nikholic*, "Digital Integrated Circuits – A Design Perspective"*, 2nd Edition, PHI, 2007.
2. David A Hodges, H. Jackson and R. A. Saleh, "*Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology"*, 3rd Edition, Tata McGraw Hill, 2007.
3. John. P. Uymera, "*Introduction to VLSI Circuits and system",* student edition, John Wiley and Sons, 2003
4. Douglas A. Pucknell, Kamran Eshraghian, " Basic VLSI design", 3rd Edition, PHI, 2003

Course Code	Course Title					Course Type
PE 611 EC	PYTHON PROGRAMMING					PE
Prerequisite	Contact hours per week			Duration of SEE (Hours)	Scheme of Evaluation		Credits
	L	T	P		CIE	SEE	
	3	-	-	3	40	60	3

Course Objectives:

- To know the basics of Programming.
- To convert an algorithm into a Python program.
- To construct Python programs with control structures.
- To structure a Python Program as a set of functions.
- To use Python data structures-lists, tuples, dictionaries.
- To do input/output with files in Python.
- To construct Python programs as a set of objects.

Course Outcomes:

1. Develop algorithmic solutions to simple computational problems.
2. Develop and execute simple Python programs.
3. Develop simple Python programs for solving problems.
4. Structure a Python program into functions.
5. Represent compound data using Python lists, tuples, dictionaries.
6. Read and write data from/to files in Python Programs

UNIT-I

Introduction to Computing and Problem Solving: Fundamentals of Computing – Computing Devices – Identification of Computational Problems – Pseudo Code and Flowcharts – Instructions – Algorithms – Building Blocks of Algorithms.

Introduction to Python Programming: Python Interpreter and Interactive Mode– Variables and Identifiers – Arithmetic Operators – Values and Types – Statements, Reading Input, Print Output, Type Conversions, The type() Function and Is Operator, Dynamic and Strongly Typed Language.

Control Flow Statements: The if, The if…else,The if…elif…else Decision Control Statements, Nested if Statement, The while Loop, The for Loop, The continue and break Statements.

UNIT-II

Functions: Built-In Functions, Commonly Used Modules, Function Definition and Calling the Function, The return Statement and void Function, Scope and Lifetime of Variables, Default Parameters, Keyword Arguments, Command Line Arguments.

Strings: Creating and Storing Strings, Basic String Operations, Accessing Characters in String by Index Number, String Slicing and Joining, String Methods, Formatting Strings.

Lists: list operations, list slices, list methods, list loop, mutability, aliasing, cloning lists, list parameters; Tuples: tuple assignment, tuple as return value; Dictionaries: operations and methods;

advanced list processing - list comprehension; Illustrative programs: selection sort, insertion sort, merge sort, histogram.

UNIT-III

Files and Exception: Text files, reading and writing files, format operator; command line arguments, errors and exceptions, handling exceptions, modules, packages; Illustrative programs: word count, copy file.

Strings: Basic String Operations, String Slicing, Testing, Searching, and Manipulating Strings

Dictionaries and Sets: Dictionaries, Sets, Serializing Objects.

UNIT-IV

Object-Oriented Programming: Classes and Objects, Creating Classes in Python, Creating Objects in Python, The Constructor Method, Classes with Multiple Objects, Class Attributes versus Data Attributes, Encapsulation, Inheritance The Polymorphism.

Functional Programming: Lambda. Iterators, Generators, List Comprehensions.

UNIT-V

GUI Programming: Graphical User Interfaces, Using the tkinter Module, Display text with Label Widgets, Organizing Widgets with Frames, Button Widgets and Info Dialog Boxes, Getting Input with Entry Widget, Using Labels as Output Fields, Radio Buttons, Check Buttons.

Suggested Readings:

1. Richard L. Halterman, "*Learning To Program With Python*", Copyright © 2011.

2. Dr. Charles R, "*Python for Everybody, Exploring Data Using Python 3*", Severance. 2016.

3. Gowrishankar S., Veena A, "*Introduction to Python Programming*", CRC Press, Taylor & Francis Group, 2019.

4. Allen B. Downey, "*Think Python: How to Think Like a Computer Scientist*", 2nd Edition, Shroff O"Reilly Publishers, 2016

Course Code	Course Title				Core/PE/OE	
PE612EC	**OPERATING SYSTEMS**				**PE**	
Pre-requisites	-		**L**	**T**	**P**	**C**
			3	-	-	3
Evaluation	**SEE**	60 Marks	**CIE**		40 Marks	

Course Objectives:	
The course is taught with the objectives of enabling the student to:	
1	To introduce the concepts of OS structure and process synchronization
2	To study different memory management strategies
3	To familiarize the implementation of file system
4	To understand the principles of system security and protection
5	To discuss the design principles and structure of Windows 7 and Linux

Course Outcomes :	
On completion of this course, the student will be able to :	
CO-1	Evaluate different process scheduling algorithms
CO-2	Describe the steps in address translation and different page replacement strategies
CO-3	Compare different file allocation methods and decide appropriate allocation strategy for given type of file
CO-4	Explain the mechanisms available in an OS to control access to resource
CO-5	Understand kernel modules, process management, memory management and file systems in linux

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	3	1	2	2	-	-	-	-	-	2	-	-
CO2	2	1	2	1	2	1	-	-	-	-	-	2	-	-
CO3	2	2	2	2	2	1	-	-	-	-	-	2	-	-
CO4	2	3	1	2	2	1	-	-	-	-	-	3	-	-
CO5	3	2	1	1	2	-	-	-	-	-	-	-	-	-

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT– I

Introduction to Operating Systems: OS structure and strategies, Process concepts, Multithreaded Programming, Process scheduling, Process synchronization, Deadlocks.

UNIT– II

Memory management strategies with example architectures: Swapping, Contiguous allocation, Paging, Segmentation, Segmentation with paging , Virtual memory management : Demand paging, Page replacement, Thrashing

UNIT– III

File system interface: File concepts, Access methods and protection. File system implementation: File system structure, Allocation methods, Directory implementation of file systems, Mass storage structures, I/O systems.

UNIT– IV

System Protection: Principles and Domain, Access Matrix and implementation, Access control and access rights, Capability based systems, Language based Protection.

System Security: Problem, Program threats, cryptography, user authentication, implementing security defenses, Firewalling, Computer security Classification

UNIT–V

Case Studies: The Linux System–Design principles, Kernel modules, Process management, Scheduling, Memory management, File systems, Input and Output, Inter process communication. Windows 7 –Design principles, System components, Terminal services and fast user switching File systems, Networking, Programmer interface

Suggested Reading:

1	Abraham Silberschatz, Peter B Galvin, Operating System Concepts, 9th edition, Wiley, 2016
2	William Stallings, Operating Systems-Internals and Design Principles, 8th edition, Pearson, 2014.
3	Andrew S Tanenbaum, Modern Operating Systems, 4th edition, Pearson, 2016.

Course Code	Course Title			Core/PE/OE	
PE613ECS	**DATA SCIENCE USING R**			**PE**	
Pre-requisites	-	**L**	**T**	**P**	**C**
		3	-	-	3
Evaluation	**SEE** 60 Marks	**CIE**		40 Marks	

Course Objectives:	
The course is taught with the objectives of enabling the student to:	
1	To learn basics of R Programming environment: R language, R- studio and R packages
2	To learn various statistical concepts like linear and logistic regression, cluster analysis, time series forecasting
3	To learn Decision tree induction and association rule mining
4	Explore the concept of decision trees and their applications in classification tasks
5	Implement clustering techniques to group similar data points together

Course Outcomes :	
On completion of this course, the student will be able to :	
CO-1	Use various data structures and packages in R for data visualization and summarization
CO-2	Use linear, non-linear regression models, and classification techniques for data analysis
CO-3	Use clustering methods and association rule mining
CO-4	Demonstrate proficiency in time series data analysis, including data reading, decomposition, and forecasting using ARIMA and exponential smoothing models in R
CO-5	Apply clustering techniques in R to group similar data points together

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	3	1	2	2	-	-	-	-	-	2	-	-
CO2	2	1	2	1	2	1	-	-	-	-	-	2	-	-
CO3	2	2	2	2	2	1	-	-	-	-	-	2	-	-
CO4	2	3	1	2	2	1	-	-	-	-	-	3	-	-
CO5	3	2	1	1	2	-	-	-	-	-	-	-	-	-

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

UNIT– I

Introduction to R: Introduction, Downloading and Installing R, IDE and Text Editors, Handling Packages in R.

Getting Started with R: Introduction, Working with Directory, Data Types in R, Few Commands for Data Exploration

Loading and Handling Data In R: Introduction, Challenges of Analytical Data Processing, Expression, Variables, Functions, Missing Values Treatment In R, Using As Operator To Change The Structure Of The Data, Vectors, Matrices, Factors, List, Few Common Analytical Tasks, Aggregation And Group Processing Of A Variable, Simple Analysis Using R, Methods For Reading Data, Comparison Of R GUI‟s For Data Input.

UNIT– II

Exploring Data In R: Introduction, Data Frames, R Functions for Understanding Data in Data Frames, Load Data Frames, Exploring Data, Data Summary, Finding the Missing Values, Invalid Values and Outliers, Descriptive Statistics, Spotting Problems In Data with Visualization.

UNIT– III

Linear Regression Using R: Introduction, Model Fitting, Linear Regression, Assumptions of Linear Regression, Validating Linear Assumption.

Logistic Regression: Introduction, What Is Regression? Introduction to Generalized Linear Model, Logistic Regression, Binary Logistic Regression, Diagnosing Logistic Regression..

UNIT– IV
Decision Tree: Introduction, What Is a Decision Tree? Decision Tree Representation In R, Appropriate Problems For Decision Tree Learning, Basic Decision Tree Learning Algorithm, Measuring Features, Hypothesis Space Search In Decision Tree Learning, Inductive Bias In Decision Tree Learning, Why Prefer Short Hypotheses, Issues In Decision Tree Learning. **Time Series in R:** Introduction, What Is Time Series Data, Reading Time Series Data, Decomposing Time Series Data, Forecasts Using Exponential Smoothing, ARIMA Models

UNIT–V
Clustering: Introduction, What Is Clustering, Basic Concepts in Clustering, Hierarchical Clustering, K-Means Algorithm. **Association Rules:** Introduction, Frequent Item set, Data Structure Overview, Mining Algorithm Interfaces, Auxiliary Functions, Sampling from Transaction, Generating Synthetic Transaction Data, Additional Measures of Interestingness, Distance Based Clustering Transaction and Association **Mining Frequent Patterns, Associations and Correlations:** Basic Concepts and Methods. Frequent Item set, Closed Item set And Association Rules. Frequent Item set: Mining Methods, Pattern Evaluation Methods

Suggested Reading:

1	Seema Acharya, "*Data Analytics using R*", McGraw Hill education
2	Nina Zumel and John Mount, "*Practical Data Science with R*", Manning Shelter Island
3	Crawley, Michael J., " The R book", John Wiley & Sons, Ltd

Course Code	Course Title						Core//PE/OE
PC651EC	**ELECTRONIC DESIGN AUTOMATION LAB**						**Core**
Pre-requisites	**Contact Hours Per Week**				**CIE**	**SEE**	**Credits**
DSD with Verilog HDL & VSLI design	**L**	**T**	**D**	**P**			
	-	-	-	2	25	50	1

Course Objectives : The course is taught with the objectives of enabling the student to:

1. To design and analyze building blocks for a Digital System using HDL platform
2. To understand a Digital System using HDL platform
3. To design and analyze CMOS circuits using back-end platform
4. To draw layout of basic CMOS circuits
5. To Design sequential and combinations circuits using building blocks **Course Outcomes :** On completion of this course, the student will be able to :

1. Demonstrate basic building blocks of a Digital System using HDL platform
2. Realize a basic Digital Systems in HDL platform
3. Demonstrate basic building blocks of a Digital System using schematic modeling
4. Demonstrate Layout design and parasitic extraction of CMOS Inverter
5. Evaluate the performance parameters of CMOS inverter at different levels of design abstractions

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	1	1	2	-	-	-	3	-	-	1	2	-
CO2	3	3	3	1	2	-	-	-	3	-	-	1	2	-
CO3	3	3	3	1	2	-	-	-	3	-	-	1	2	-
CO4	3	3	3	2	2	-	-	-	3	-	-	1	2	-
CO5	3	3	3	2	2	-	-	-	3	-	-	1	2	-

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

Experiment-I

Design and Write a Verilog HDL code for BCD to 7-segment decoder for LED and LCD displays and verify

Experiment-II

Design a 4-bit shift right barrel shifter using 2:1 Mux
Design a 4-bit shift left barrel shifter using 2:1 Mux
Verify both the designs with a test bench.

Experiment-III
Design a sequence detector for a given sequence in Verilog HDL and verify its function through a test bench and write the output to a file.

Experiment-IV
Design a 4-bit CLA and develop HDL code using Generate Loop statements
Design a 4X4 unsigned array Multiplier and develop a HDL code using Generate Loop statements. Verify both the designs with attest bench.

Experiment-V
Develop a Verilog HDL code for SR and T flip flops with synchronous reset
Develop a Verilog HDL code for JK and D flip flops with asynchronous reset Verify them with a suitable test bench

Experiment-V
Design an N-bit shift register with asynchronous reset and synchronous load/shift controls to operate in the following modes, namely PIPO, SIPO, SISO, PISO. Develop a Verilog HDL code and verify the operation with a test bench

Experiment-VI
Draw schematic of all CMOS basic gates and simulate using Cadence Schematics tool

Experiment-VII
Develop basic Building blocks as MUX, Half adder, Full adder, Encoder using CMOS gates in Cadence and verify

Experiment-VIII
Develop a 4-bit Carry look ahead adder and a Carry Bypass adder using Cadence Schematics and verify.

Experiment-IX
Develop a 4-bit Array multiplier with CLA as end accumulator and verify .

Experiment-X
Develop a 4-bit Carry save multiplier and verify its function using cadence tool.

Experiment-X
Design and analyze the following CMOS circuits: Inverter using static, ratioed, dynamic and domino logic styles

Experiment-XI
Design a CMOS inverter and obtain VTC using Cadence Tools

Experiment-XII

Draw the layout and evaluate the performance of CMOS Inverter and two-input CMOS NAND gate

SUGGESTED READING:

1. Samir Palnitkar, *"Verilog HDL A Guide to Digital Design and Synthesis,"* 2nd Edition, Pearson Education, 2006
2. Ming-Bo Lin, *"Digital System Designs and Practices: Using Verilog HDL and FPGA*," Wiley India Edition, 2008
3. David A Hodges, H. Jackson and R. A. Saleh, "*Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology"*, 3rd Edition, Tata McGraw Hill, 2007.

Course Code	Course Title						Core//PE/OE
PC652EC	**MICRO-CONTROLLERS LAB**						**Core**
Pre-requisites	**Contact Hours Per Week**				**CIE**	**SEE**	**Credits**
Micro-Controllers and Interfacing	**L**	**T**	**D**	**P**			
	-	-	-	2	25	50	1

Course Objectives : The course is taught with the objectives of enabling the student to:

1. Discuss Basic 8051 Assembly Language Programming
2. Discuss Basic ARM Programming
3. Discuss Timer & Interrupt Programming
4. Discuss Real time Interfacing using 8051 and ARM

Course Outcomes : On completion of this course, the student will be able to :

1. To understand Keil IDE for simulating 8051 and ARM7
2. To write basic assembly language programs for arithmetic and logical operations using 8051
3. To program Timers, serial communication and Interrupts using 8051
4. To interface ADC,DAC, LED, Seven Segment display, Stepper motor using 8051 and ARM LPC2148
5. To Write programs for PWM, sensor interfacing using LPC 2148

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	1	1	2	2	3	-	-	-	1	-	1	1
CO2	1	2	2	2	3	-	-	-	1	-	1	1
CO3	1	2	3	3	3	-	-	-	1	-	1	1
CO4	1	2	3	3	3	-	-	-	1	-	2	2
CO5	1	2	3	3	3	-	-	-	1	-	2	2

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively.

Experiment–I

Programs for Basic Arithmetic and Logical Operations using 8051

Experiment–II

Program for Sorting, Searching an array using 8051

Experiment–III

Generating Square wave form using Timers in 8051

Experiment–IV

Program for serial communication using on-chip UART 8051

Experiment–V
Design of a Digital Clock using Timers/ Counters in 8051 **Experiment–VI**
Design an interface to connect LEDs to 8051 and write a program for blinking LEDs

Experiment–VII
Design a Seven Segment Display interface using 8051and write a program to display varuios numbers

Experiment–VIII
Interface ADC to 8051 and interface DAC to 8051, and write programs to generate Triangle and square waves

Experiment–IX
Interface Stepper Motor using 8051, program it to rotate in clockwise and anti clockwise directions

Experiment–X
Interface DIP Switches and LEDs to ARM, program to blink LEDs on switch press

Experiment–XI
Design an interface to connect 16x2 LCD using ARM

Experiment–XII
Interface and rotate DC Motor using ARM

Experiment–XIII
Interfacing RTC Using I2C in ARM

Experiment–XIV
Using on chip Timers/Counters for PWM Generation using ARM

SUGGESTED READING:

1. Mohammad Ali Mazidi, Rolin D McKinley, Janice G Mazidi, The 8051 Microcontroller and Embedded Systems, Second Edition, Prentice Hall
2. Kenneth J Ayala, The 8051 Micro Controller: Architecture, Programming and Applications
3. Jonathan W. Valvano, " Introduction to ARM CORTEX-M Microcontrollers", Volume 1, fifth Edition, June 2024
4. Dr. Yifeng Zhu, "Embedded Systems with ARM Cortex-M micro controllers in Assembly Language ad C".

Course Code	Course Title						Core//PE/OE
PW653EC	**MINI - PROJECT**						**Core**
Pre-requisites	**Contact Hours Per Week**				**CIE**	**SEE**	**Credits**
	L	**T**	**D**	**P**			
	-	-	-	6	50	-	3

Course Objectives : The course is taught with the objectives of enabling the student to:

1. To enhance practical and Professional skills
2. To expose the students to industry practices and team work.
3. To encourage students to work with innovative and entrepreneurial ideas.

Course Outcomes : On completion of this course, the student will be able to :

1. Conceive a problem statement either from rigorous literature survey or from the requirements raised from need analysis.
2. Design, implement and test the prototype/algorithm in order to solve the conceived problem.
3. Write comprehensive report on mini project work

Guidelines:

1. The mini-project is a team activity having 3-4 students in a team. This is mechanical product design work/ manufacturing process with a focus on mechanical system design/manufacturing process.
2. The mini project may be a complete hardware or a combination of hardware and software. The software part in mini project should be less than 50% of the total work.
3. Mini Project should cater to a small system required in laboratory or real life.
4. It should encompass components, devices, with which functional familiarity is introduced.
5. After interactions with course coordinator and based on comprehensive literature survey/ need analysis, the student shall identify the title and define the aim and objectives of mini-project.
6. Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and submit the proposal within first week of the semester.
7. The student is expected to exert on design, development and testing of the proposed work as per the schedule.
8. Art work and Layout should be made using CAD based software.
9. Completed mini project and documentation in the form of mini project report is to be submitted at the end of semester.